IN THE SPECIFICATION:

Please amend the specification as follows:

Please replace paragraphs [001], [012], [013], [014], [031], [033], [038], [039], [077], and [082], with the following paragraphs:

[001] U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, is hereby incorporated by reference.

[012] Because status information is represented by flags that are stored in floating point status registers, implicit serialization is required. It would be desirable to indicate a status of an operand or result within the operand or result, rather than representing the status by flags stored in floating point status registers. U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, describes a floating point unit that encodes floating point status information in the results generated by the floating point unit, which obviates the need for implicit serialization. The floating point unit includes a plurality of functional units, including an adder unit, a multiplier unit, a divider unit, a square root unit, a maximum/minimum unit,

a comparator unit and a tester unit, all of which operate under control of functional unit control signals provided by a control unit.

[013] Further, U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, discloses seven exemplary floating point formats including a zero format, an underflow format, a denormalized format, a normalized nonzero format, an overflow format, an infinity format, and a NaN format. Still further, U.S. Patent No. 6,131,106 ("the '106 patent"), issued October 10, 2000 and entitled "System And Method For Floating Point Computation In Delimited Floating Point Representation," assigned to the assignee of the present application, which is hereby incorporated by reference, discloses a delimited format.

[014] Regarding a logarithm unit, IEEE Std. 754 specifies a logarithm function that essentially generates the contents of the exponent field of a floating point number minus an exponent bias as a result. However, this result may not be mathematically accurate for all formats. It is desirable to provide a logarithm unit that generates a mathematically accurate integer part of a logarithm of an absolute value of an operand for all formats including formats provided by IEEE Std. 754, U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, and U.S.

Patent No. 6,131,106. Further it is desirable to provide a logarithm unit that encodes floating point status information in the results generated by the logarithm unit. Still further, if status information is encoded in the operand, it is desirable to provide a logarithm unit that preserves the status information in the result.

[031] More specifically, if the operand 200 is in a NaN format according to related U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, then the result generator 140 may generate a result in the NaN format having the same sign and status information as the operand 200. If the operand 200 is in a NaN format according to IEEE Std. 754, then the result generator 140 may generate a result in the NaN format having the same sign as the operand 200 and may generate at least one signal indicating status information (e.g., divide-by-zero).

[033] If the operand 200 is in an infinity format according to related U.S. Patent Application Serial No. 10/035,747, then the result generator 140 may generate a result additionally having the same status information as the operand 200.

[038] Fig. 3 illustrates an exemplary embodiment of a logarithm unit 100a that may be used when the floating point operand 200 stored in the operand buffer 110 may be in a format according to related U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point

System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application.

[039] Fig. 7 illustrates the zero format 710, the underflow format 720, the denormalized format 730, the normalized nonzero format 740, the overflow format 750, the infinity format 760, and the NaN format 770, as disclosed in related U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application. As shown in Fig. 7, in the zero format 710, the exponent field bits, $e_{msb} \cdots e_{lsb}$, and the fraction field bits, $f_{msb} \cdots f_{lsb}$, are all binary zeros. In the underflow format 720, the exponent field bits, $e_{msb} \cdots e_{lsb}$, are all binary zeros, the twenty-two most significant fraction field bits, $f_{msb} \cdots f_{lsb+1}$, are all binary zeros, and the least significant fraction field bit, f_{lsb}, is a binary one.

[077] Fig. 4 illustrates an exemplary embodiment of an logarithm unit 100b that may be used when the floating point operand 200 stored in the operand buffer 110 may be in a format according to U.S. Patent Application Serial No. 10/035,747, filed on even date herewith in the name of Guy L. Steele Jr. and entitled "Floating Point System That Represents Status Flag Information Within A Floating Point Operand," assigned to the assignee of the present application, but instead of the described denormalized format, the operand 200 may be in a delimited format according to U.S. Patent No. 6,131,106.

Referring now to Fig. 4, the logarithm unit 100b is similar to the logarithm unit 100a described above, except that it includes a count trailing zeros circuit 152 instead of a count leading zeros circuit 52 to provide the value n.

[082] Further, the above description of the logarithm unit 100 has been in reference to operands formatted according to U.S. Patent Application Serial No. 10/035,747, U.S. Patent No. 6,131,106, and IEEE Std. 754. However, the logarithm unit 100 may be adapted to receive a floating point operand having a different format. Adapting the logarithm unit 100 to receive a floating point operand having a different format will be obvious to those of ordinary skill in the art.